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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,908	08/26/2003	Darren Lane Anand	BUR920030088US1	1907

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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,908	ANAND ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13 and 14* is/are allowed.

6)☒ Claim(s) *1-12 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are present for this Response to applicants instant Response.

Claim Objections

Acknowledgment is made that the claim objections noted to applicant have been overcome by the amendments to the claims.

Response to Arguments

Applicant's arguments filed 4/24/2006 have been fully considered by the Examiner. Applicant's arguments with respect to claims 1-12 and 15-20 have been considered but are moot in view of the new ground(s) of rejection in addition to Multiplexers ("Multiplexers and Demultiplexers"), Maejima (US Patent 6639848) Esposito (US Patent 4066882), along with the understanding and interpretation of the claims as they read.

With respect to the 35 USC 112 Claim Rejections, the applicant has not provided corrections or explanations that would provide understanding to the Office as to what applicant is particularly pointing out and distinctly claiming as the invention. The claims still are indefinite and fail to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner therefore maintains the 35 USC 112 rejections. Examiner notes that further explanation to the particulars to the 35 USC 112 rejections are disclosed below.

With respect to Applicant's arguments to the 35 USC § 102 and 103 rejections in view of the 35 USC 112 rejections applicant argues the references cited do not teach:

i. A first latch having a single data input port and a single clock input port and an output port.

ii. A second latch also having a single data input port and a single clock input port and an output port.

iii. Means for ... selection of a scan chain input at said first latch and said second latch.

iv. Means ... selection of a shift chain input at said first latch and said second latch.

v. Wherein a selection of the scan chain input ... occurs exclusive of selection of the shift chain input..., and wherein said single data input latches provides functionality of latches that support multiple inputs.

As per applicant's arguments i-v, examiner would like to direct the applicant specifically to arguments iii and iv in view of arguments i and ii, wherein the first issue of failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention resides. It is unclear to the examiner how "at," the first and second latches a "selection," such as described within arguments iii and iv can take place between two different inputs (shift chain and scan chain) with two different clocks (first and second). The latches as claimed in arguments i and ii only accepts a single data input and a single clock input at the single data input port and single clock input. In view of this issue examiner has indicated within the first action for the remainder of this action (response to applicants instant response) it is unclear how a single input latch has two distinct inputs (scan chain and shift chain, first and second clock) at the single

data input port and single clock input port respectively. Appropriate correction or explanation was and is required for understanding.

As per applicant's arguments i-v, examiner would like to direct the applicant specifically to argument v in view of arguments i-iv, wherein the second issue of failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention resides. It is unclear what "means" performs the "selection" as described within argument v in view of arguments iii and iv, wherein a scan chain or shift chain input is selected and passed to the single data input port of said first and second latches, and wherein the selection of one input is exclusive of the other. Examiner points out that a means that one of ordinary skill in the art at the time the invention was made would recognize as well know for selecting between the scan chain and shift chain inputs prior to input to the single data input port latches was provided within the circuit since one was not claimed but required in view of the claim.

The 35 USC 112 rejections are maintained and have been given further explanation so as to better explain the issues with the claims as they read. Applicant strongly advised to correct the 35 USC 112 issues, which render the claims indefinite.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, it is unclear to the examiner as described above both, how a selection can take place "at" the first and second latches wherein only a single input (data and clock) is provided to the latches and what the "means" is for performing a "selection" prior to passing to the single data input fort of said first and second latches. In view of this rejection for claim 1, for the purposes of examination the single input latches will be assumed to be a standard multiplexer. Appropriate correction or explanation is required for understanding if this is not applicants intended subject matter, which is to be regarded as the invention.

Claims 2-11 are dependent on claim 1 and therefore also inherit the 35 USC 112, second paragraph issues of the independent claims and may not be further considered on their merits.

Claim 11 recites the limitation "said semiconductor device" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that within claim 11 or claims that claim 11 is dependent on is a semiconductor device disclosed. Appropriate correction or explanation is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 2, 3, 8, and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by "Multiplexers and Demultiplexers" (hereafter referred to as Multiplexers).

1. As per claim 1, Multiplexers teaches an input circuit (top two MUXes in the figure on page 7 of 10) for providing separate scan and shift paths (top two figures on page 2 of 10) for a device (bottom MUX in the figure on page 7 of 10) untilizing single input latches (top two MUXes in figure on page 7 of 10, top figures on page 2 of 10), said circuit comprising:

A first latch (top left MUX on page 7 of 10) having a single data input port (0 and 1) and single clock input (C) port and an output port (Z);

A second latch (top right MUX on page 7 of 10) having a single data input port (0 and 1) and a single clock input port (C) and an output port (Z);

A first clock input (C0 as a "0") that enables selection of a scan chain input at said first latch and said second latch (X0 and X2 respectively);

A second clock input (C0 as a "1") that enables selection a shift chain input at said first latch and said second latch (X1 and X3 respectively); and

Wherein a selection of a scan chain input (X0 or X2) for passing to said input ports ("0") of said latches occurs exclusive of selection of a shift chain input (X1 or X3) for passing to said input ports ("1"), and vice versa, and wherein said single input latches (top two MUXes in the figure on page 7 of 10) provide functionality of latches that support multiple inputs.

2. As per claim 2, Multiplexers teaches the input circuit described above further comprising:

Means for receiving said scan chain and said first clock input (figure on page 7 or 10); and

Means for receiving said shift chain input and said second clock input (figure on page 7 of 10).

3. As per claim 3, Multiplexers teaches the input circuit described above further comprising:

Means for receiving a data signal (X0, X1, X2, X3) at a port ("0", "1") of said latches (top two MUXes in the figure on page 7 of 10), wherein said data signal is one of a scan chain input (X0, X2) and a shift chain input (X1, X3);

Means for accepting the scan chain input into said latches (figure on page 7 of 10) to commence a scan chain operation (top right figure on page 2 of 10) within said device (bottom MUX in figure one page 7 of 10) then a first clock signal (C1) is on ("1"); and

Means for accepting the shift chain input into said latches (figure on page 7 of 10) to commence a shift chain operation (top left figure on page 2 of 10) within said device (bottom MUX in figure one page 7 of 10) when a second (C1), different (C1 not C0) clock signal is on ("1"), wherein only one clock signal is on at a time and both said scan chain operation and shift chain operation are supported by said single input latches (figure on page 7 of 10).

4. As per claim 8, Multiplexers teaches the input circuit as described above as per claim 1, wherein the first clock signal (C0) and second clock signal (C1) each provide a select signal ("0" or "1") for respectively receiving either said scan chain input or said shift chain input into said latches (see figures on pages 2 of 10, and 7 of 10), wherein

further, the selected input provides a respective scan chain or shift chain operation to be propagated through the device (bottom MUX in figure on page 7 of 10).

5. As per claim 10, Multiplexers teaches the input circuit as described above as per claim 1, wherein the device is a semiconductor device and said input circuit (top two MUX in figure 7 of 10) is fabricated on said semiconductor device (see figure on page 7 of 10).

Claim Rejections - 35 USC § 103

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers as applied to claim 3 above, and further in view of Esposito (US Patent 4066882).

6. As per claims 4 and 5, Multiplexers teaches the input circuit described above as per claim 3.

Multiplexers does not specifically teach the means for accepting scan chain and shift chain inputs including first level respective NAND gates with respective first and second clock signal inputs which yield respective scan chain and shift chain NAND outputs respectively which are the inputs of a second level NAND gate that yields a subsequently NANDed two-tiered NAND result.

However in an analogous art, Esposito teaches the two-tiered input NAND input means (see figures 11d(7), 11d(6), 10d(4), 10c(6) and 10b(7)) that would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the means for accepting scan chain and shift chain inputs along with selecting either as an output.

Therefore, one would be motivated to have used Esposito's two tiered input NAND input means since NAND gates and two-tiered NAND gate configurations are standard logic for input means as shown by Esposito.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers.

7. As per claim 6, Multiplexers teaches the input circuit described as per claim 1.

Multiplexers does not specifically teach the input circuit wherein the second clock input is ANDed with a shift input to yield a shifted second clock input that is utilized as the second clock input for selection of the shift chain input.

However those of ordinary skill in the art at the time the invention was made would recognize that what Multiplexers does not specifically teach as described above is well known in the art.

Therefore, one would be motivated to shift the second clock input by ANDing it with a shift input when it is desired to delayed an input clock or produce a additional clock input, delayed by a set amount of time in-order to perform additional procedures; AND gates are standard logic that is used to shift signals throughout circuitry.

8. As per claim 7, Multiplexers teaches the input circuit described above as per claim 1.

Multiplexers does not specifically teach the input circuit further comprising an OR gate having inputs of said first clock and a result of an ANDing of said second clock with a shift input, wherein an output of said OR gate is utilized as the clock input of said latches (multiplexers).

However those of ordinary skill in the art at the time the invention was made would recognize that Multiplexers does not specifically teach as described above is well known in the art.

Therefore, one would be motivated to OR the first clock with the shifted second clock signal in-order to produce a faster or slower oscillating clock in-order to perform additional procedures; OR gates are standard logic that is used to produce signals throughout circuitry.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art (AAPA).

9. As per claim 9, Multiplexers teaches the input circuit described above as per claim 1.

Multiplexers does not specifically teach wherein the latches are LSSD latches.

However those of ordinary skill in the art at the time the invention was made would recognize that the use of a LSSD latch in place of a standard multiplexer is well known, since both the LSSD and standard MUX perform the same function of selecting and input to be provided as an output.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to use an LSSD latch in place on the standard MUX within Multiplexers wherein it would reduce the size and power consumption, while increasing the speed of the circuitry without compromising the functionality of the circuit.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers as applied to claim 9 above, and further in view of Maejima (US Patent 6639848).

10. As per claim 11, Multiplexers teaches the input circuit as described above as per claim 9.

Multiplexer does not specifically teach the input circuit wherein the device is an eFuse device.

However in an analogous art, Maejima teaches that eFuse devices need input circuitry (see figures 2, 6, 8, 11, 12, and 14).

Therefore one would be motivated to combine the teaches of Multiplexers and Maejima in-order to minimize circuitry needed to implement different functions within the eFuse device.

Claim 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Multiplexers and Demultiplexers" (hereafter referred to as Multiplexers) and Applicants Admitted Prior Art (AAPA).

11. As per claim 12, Multiplexers as described about as per claim 1 teaches in input circuit the enables a scan only latch to be utilized to dynamically select from among a scan chain path and a shift chain path being inputted to said device utilizing a series of input clock signals operating as MUX selects for the scan only latches to select either said scan chain path or said shift chain path for passing through said device (refer above as per claim 1). Examiner notes that this same input circuit is disclosed within AAPA (0008-0011 along with figure 1). Additionally, AAPA teaches that testing a device

may involve selectively blowing fuses within the device by passing an electrical current through a fuse link, depending on the design of the fuse/device, and that generally known in the art are more then one method of selecting which fuses are blown (0005).

Multiplexers nor AAPA specifically teach serially connected eFuse circuitry comprising:

AND logic having two inputs and an output; and

A multiplexer (MUX) having a first input, a second input, a select input, and a MUX output, wherein said output of said AND logic is coupled to said select input of said MUX.

However those of ordinary skill in the art at the time the invention was made would recognize that using a standard, two input, single output AND logic gate with its output connected to the selection input of a two input, single output, single selection input MUX is well known. Examiner notes that AAPA teaches of an AND logic gates output used as a control input for circuitry within a circuit (see 0009).

Therefore one of ordinary skill in the art would have been motivated in use the output of a standard AND logic gate to control a standard MUX wherein a number of signals need to be in a particular state for the MUX to select a particular input as its output and subsequent input to other circuitry when a design or method calls for such a condition.

Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Multiplexers or AAPA and as evidenced by Esposito (US Patent 4066882).

12. As per claims 15-20, Multiplexers as described above as per claim 1 teaches an input circuit the enables a scan only latch to be utilized to dynamically select from among a scan chain path and a shift chain path being inputted to said device utilizing a series of input clock signals operating as MUX selects for the scan only latches to select either said scan chain path or said shift chain path for passing through said device (refer above as per claim 1). Examiner notes that this same type of input circuit is disclosed within AAPA (0008-0011 along with figure 1).

Multiplexers nor AAPA specifically teach wherein the input circuit is a two-tiered NAND gate circuit configured to output to a circuit either one or two data inputs dependent on two clock inputs.

However to would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a MUX type circuitry out of NAND gate logic units wherein clock inputs determine which data input is outputted from the circuitry since the examiner takes official notice of the equivalence of the two tired NAND gate configuration and a MUX circuit for their use in the choosing/selecting/determining art and the selection of either of these known equivalents to select from a number of inputs as an output would be within the level of ordinary skill in the art.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to use the equivalent two-tiered NAND gate circuit input means since NAND gates and two-tiered gate configurations are standard logic for input means as evidenced by Esposito (see figures 11d(7), 11d(6), 10d(4), 10c(6) and 10b(7)).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
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